EE105
Microelectronic Devices and Circuits:
MOS Large Signal Model and Bias Circuits

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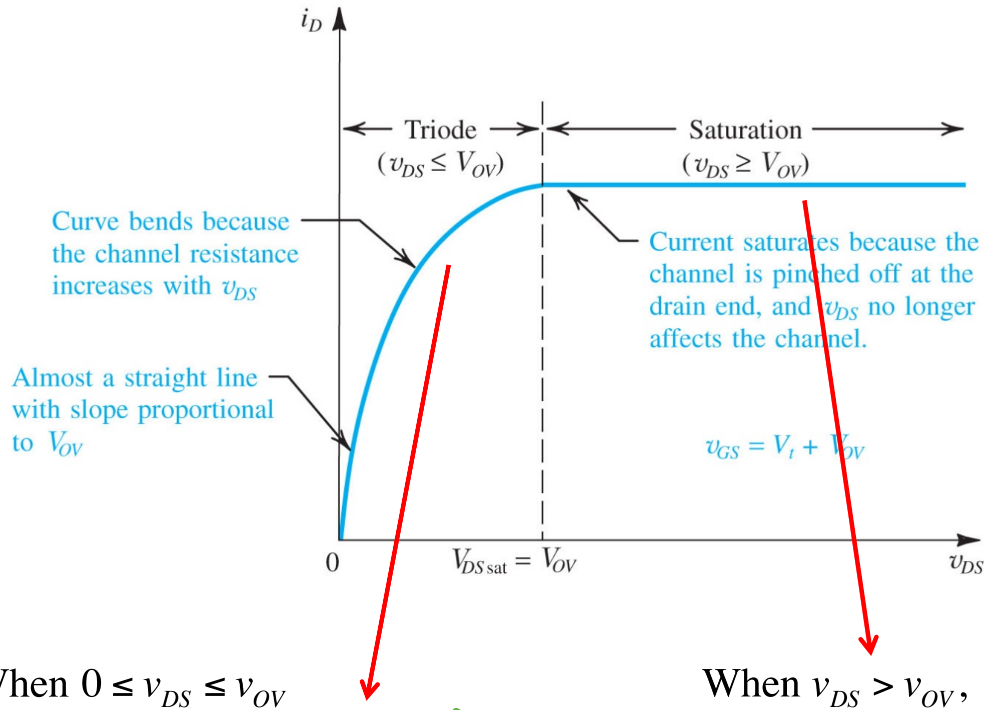
Saturation Region ($v_{DS} > v_{OV}$)



When $0 \le v_{DS} \le v_{OV}$

$$i_D = \mu_n C_{ox} \frac{W}{L}\left(v_{OV} v_{DS} - \frac{1}{2} v_{DS}^2\right)$$

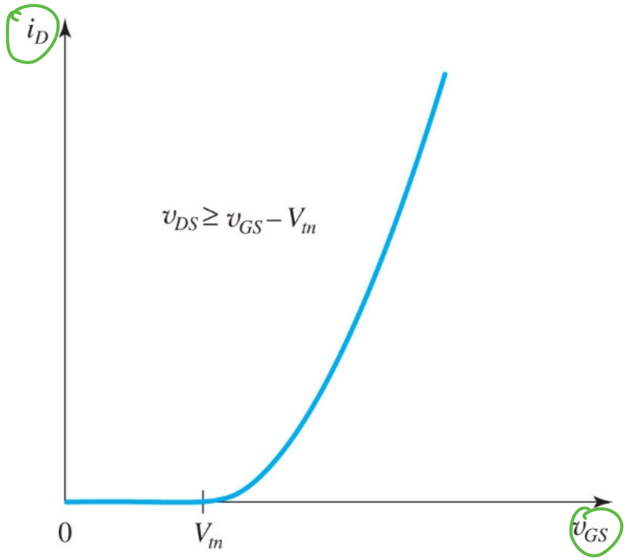
This is called the "Triode Region"

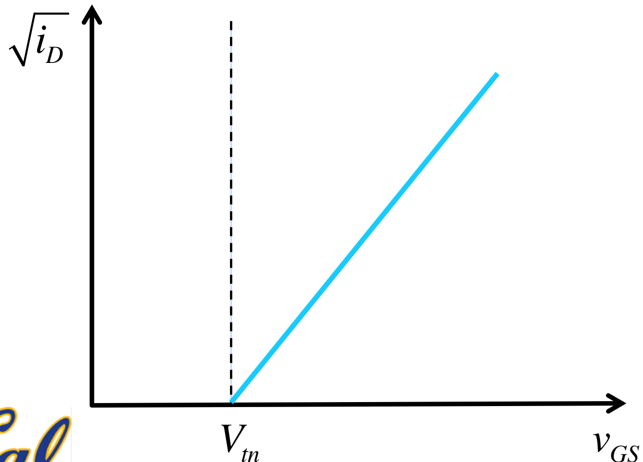
When $v_{DS} > v_{OV}$,

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} v_{OV}^2$$

This is called "Saturation Region"

Drain Current vs Gate Voltage





In Saturation Region

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_{tn})^2$$

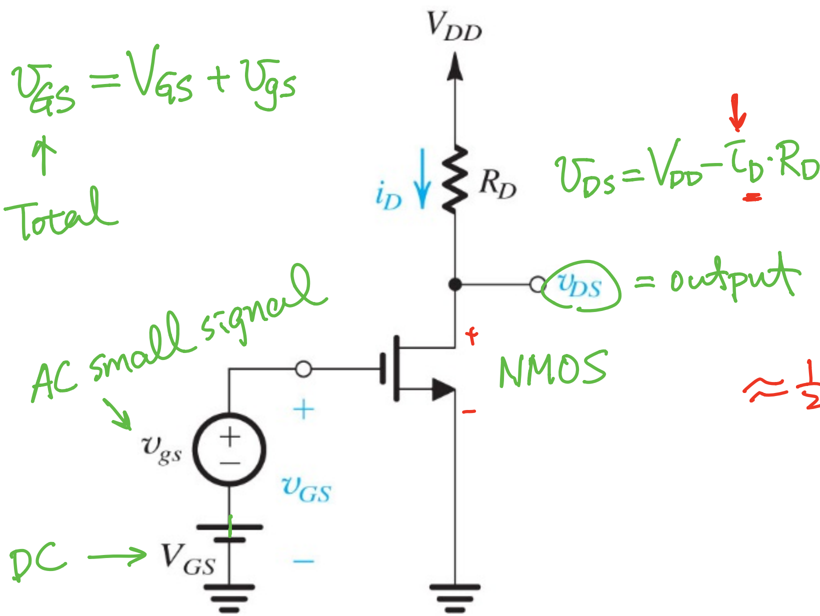
To experimentally determine V_{tn} :

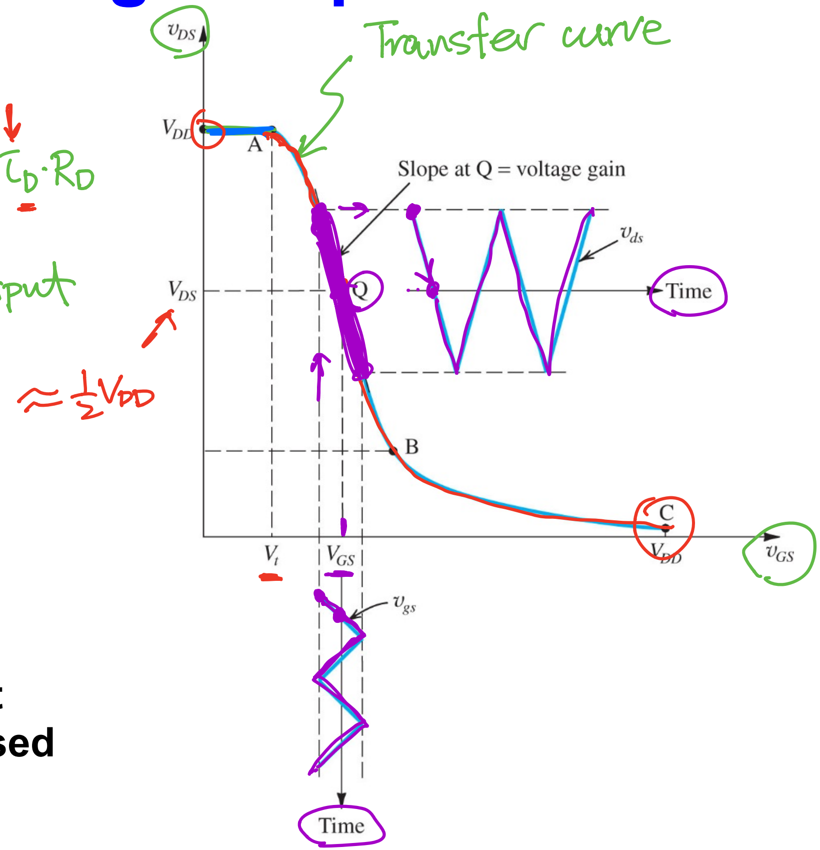
Measure and plot $\sqrt{i_D}$ versus v_{GS}

$$\sqrt{i_D} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}(v_{GS} - V_{tn})$$

V_{tn} = intercept with horizontal axis

Analog Voltage Amplifier



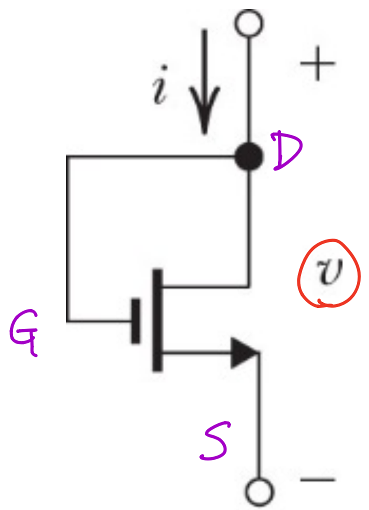


- **DC bias at Quiescent (Q) point**
- **Small-signal input superimposed on a DC bias voltage**
- **Symbol used in this course:**

$$v_{GS} = V_{GS} + v_{gs}$$

- **Need to know the transistor's I-V characteristics to find the voltage gain (and other properties of the amplifier)**

Diode-Connected Transistor



With Gate connected to Drain, it becomes a 2-terminal device.

This is called "diode-connected transistor"

In this configuration, the transistor is always in "Saturaiton".

Its I-V relationship is:

$$i = I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2$$

$$v_{GS} = v_{DS} = v$$

$$v_{OV} = v_{GS} - V_{tn} = v - V_{tn}$$

$$i_{D,sat} = i_D = i = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v - V_{tn})^2$$

$v_{OV} = v_{DS} - V_{t,n}$

$= v - V_{t,n}$

First Question:

Is FET in triode or saturation?

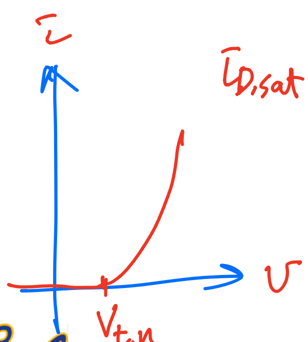
Assume ~~triode~~ → test.

v_{DS} : $v_{OV} = v_{GS} - V_{t,n}$ (+)

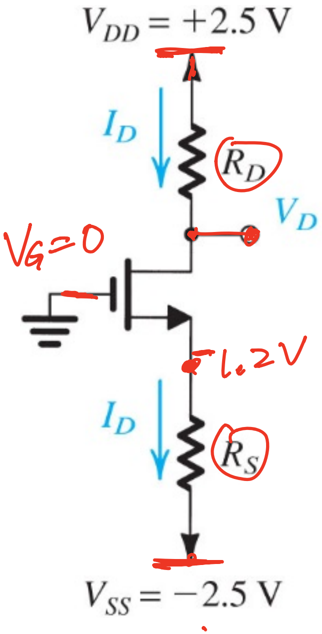
$v_{DS} = v_{GS} > v_{OV}$

$D = G$

⇒ FET is in Saturation



Example Circuit (1)



Design Problem: → Need set I_D, V_{DS}

Determine R_S and R_D such that the NMOS is biased at $I_D = 0.4mA$ and $V_D = 0.5V$. The NMOS has $V_t = 0.7V$, $\mu_n C_{ox} = 100\mu A/V^2$, $L = 1\mu m$ and $W = 32\mu m$.

Choose $V_D = 0.5V$

$I_D = 0.4mA = \frac{V_{DD} - V_D}{R_D}$

Solution:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5k\Omega$$

Need MOSFET in Saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{OV}^2 = 0.4mA \text{ --> } v_{OV} = 0.5V$$

(channel length modulation can usually be ignored when solving DC bias)

$$v_{GS} = V_t + v_{OV} = 0.7 + 0.5 = 1.2V$$

$$V_G = 0 \text{ (grounded) --> } V_S = -1.2V$$

$$R_D = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25k\Omega$$

$V_{GS} = v_{OV} + V_{t,n}$
$= 0.5 + 0.7 = 1.2V$

$R_S = \frac{(1.2 - (-2.5))V}{0.4 mA}$